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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/010,082	12/19/2007	6038195	38512.11	3316

7590 02/15/2008

EXAMINER

NEIL A. STEINBERG, ESQ
RAMBUS INC.
2465 LATHAM STREET
MOUNTAIN VIEW, CA 94040

ART UNIT	PAPER NUMBER

DATE MAILED: 02/15/2008

Please find below and/or attached an Office communication concerning this application or proceeding.

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DAVID M. O'DELL
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MAILED

FEB 15 2008

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/010,082*.

PATENT NO. *6038195*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/010,082	6038195	
	Examiner	Art Unit	
	Ovidio Escalante	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *19 December 2007* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO/SB/08, c)☒ Other: *Decision*

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

Ovidio Escalante
CRU Examiner
Art Unit: 3992

cc:Requester (if third party requester)

DECISION GRANTING *EXPARTE* REEXAMINATION

1. A substantial new question of patentability affecting claims 1-24, 27 and 32-37 of United States Patent Number 6,038,195 (Farmwald et al. patent) is raised by the request for *exparte* reexamination.

2. The instant patent issued March 14, 2000 based on US Patent Application Ser. No. 09/196,199, filed November 20, 1998 as a continuation of U.S. application 08/798,520, filed February 10, 1997, now U.S. Patent 5,841,580 as a division of U.S. application 08/448,657, filed May 24, 1995, now U.S. Patent 5,638,334, as a division of U.S. application 08/222,646, filed on March 31, 1994, now U.S. Patent 5,513,327 as a continuation of U.S. application 07/954,954, filed September 30, 1992, now U.S. Patent 5,319,755 as a continuation of U.S. Application 07/510,898, filed April 18, 1990.

References Cited in the Request

3. Page 6 of the Request identifies the following printed publications as providing teachings relevant to the claims of the '195 Farmwald patent

Exhibit B	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Release 4, **November 1993 (the JEDEC Standard)**.
Exhibit C	U.S. Patent No. 5,590,086 to Park et al. (**Park**) issued on **December 31, 1996**.
Exhibit D	US Patent 5,361,277 to **Grover**, issued **November 1, 1994** (Grover).
Exhibit E	UK Published Patent App. No. GB 2197553 to Lofgren et al. **published May 18, 1988 (Lofgren)**.
Exhibit F	Johnson et al., A Variable Delay Line PLL for CPU - Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, **published October 1988 ("Johnson")**

Exhibit G	Intel Corporation iAPX 432 Interconnect Architecture Reference Manual, **published 1982 (the iAPX Manual).**
Exhibit H	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), **published March 1983 (the iAPX Specification).**
Exhibit I	US Patent 4,480,307 to Budde et al. **(Budde)** issued **October 30, 1984.**
Exhibit J	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs, **published in January 1989 (Rau).**

Detailed Explanation of How the Cited Prior Art is Applied to Every Claim for Which Reexamination is Requested.

Alleged Anticipatory SNQs Based on Intervening References

1. The JEDEC Standard is asserted as rendering claims 1-3,5-8,10-13,15-18,20-24,27 and 35-37 anticipated.

2. US Patent 5,590,086 to Park et al. is asserted as rendering claims 1-3, 5-8, 10-13, 15-18, 20-24, 27 and 32-37 anticipated

Alleged Anticipatory SNQs based on Prior Art

3. iAPX Manual is asserted as rendering claims 1,3,5-8,10-11,15-18,20,23-24,27 and 32-37 anticipated.

4. US Patent 4,480,307 to Budde et al. is asserted as rendering claims 1,3,5-8,10-11,15-18,20,23-24,27 and 32-37 anticipated.

Alleged Obviousness SNQs Based on Intervening References

5. The JEDEC Standard in view of Grover, Lofgren or Johnson is asserted as rendering claims 4,9,14 and 19 obvious.

6. Park in view of Grover, Lofgren or Johnson is asserted as rendering claims 4, 9, 14 and 19 obvious.

Alleged Obviousness SNQs based on Prior Art

7. iAPX Manual in view of iAPX Specification is asserted as rendering claims 3, 20, 35 and 37 obvious.

8. iAPX Manual in view of Grover, Lofgren or Johnson is asserted as rendering claims 2,4,9,12-14,19 and 21-22 obvious.

9: Budde in view of Grover, Lofgren or Johnson is asserted as rendering claims 2, 4, 9, 12-14, 19 and 21-22 obvious.

10. Budde in view of Rau is asserted as rendering claims 1, 5, 8 and 18 obvious.

Alleged anticipatory issues 1-2 and alleged obviousness issues 5-6 comprise art that fails to antedate the original filing date of a patent Application of which the instant '195 Patent claims benefit. This issue will be discussed *infra*.

Priority Issues Related to Oath or Declaration

The Requester on pages 9-10 of the request asserts that the instant '195 Patent should not be accorded the filing date of the original '580 Parent Patent. This is due to Requester's allegation that the parent Patent of the instant '195 Patent failed to present a proper oath or declaration specifically referring to the initial preliminary amendment filed with the initial application.

The issue of whether certain claims of the '195 patent are not entitled to an earlier effective filing date because such claims contain elements that are argued to have been supplied by a preliminary amendment that was not covered by the 37 CFR 1.63 declaration of record will not be decided in this Order. As discussed below, the request is deemed to establish a substantial new question of patentability for the '195 claims on other bases. Therefore, the Office will accept jurisdiction over the '195 on those "more conventional" SNQs. The question raised with respect to lack of entitlement to an earlier effective filing date because the 37 CFR 1.63

declaration filed in the application that matured into the '195 patent did not "cover" the preliminary amendment that added support for certain claim features is reserved for the first Office action on the merits.

Priority Issues Related to the References/Instant Claims

The MPEP states "to be entitled to an earlier priority date or filing date under 35 U.S.C. 119, 120, or 365(c), each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure." MPEP 2163 II.A.3(b).

> A rejection may be made in reexamination proceeding based on an intervening patent when the patent claims under reexamination, under 35 U.S.C. 120, are entitled only to the filing date of the patent under reexamination. Specifically:
>
> > Rejections on art in reexamination proceedings may only be made on the basis of prior art patents or printed publications. See MPEP § 2258 and § 2258.01 for a discussion of art rejections in reexamination proceedings based on prior art patents or printed publications.

(MPEP § 2258.1.C, Scope of Ex Parte Reexamination) (emphasis added).

To be entitled to priority under 35 U.S.C. 120, the previously filed application of the parent patent must comply with 35 U.S.C. 112, first paragraph. Specifically:

> An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, ms though fled on the date of the prior application[.]

(35 U.S.C. 120, Benefit of Earlier Filing Date in the U.S.)

> 35 U.S.C. 112, 1st paragraph, in turn, requires the written description of the application describe the claimed invention with sufficient particularity that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-17 (Fed. Cir. 1991). See also MPEP § 2163.

Thus, in reexamination, an analysis of the instant Patent's effective priority date is proper.

Analysis

4. Third Party alleges on pp. 11-19 of the request a number of features in the claims that are allegedly not supported by the original disclosure of the '580 parent patent under 35 U.S.C.

§112. The references that predate November 20, 1998, for the purposes of this proceeding as it currently stands thus may potentially raise a SNQ over claims of the instant Patent.

The request on page 11, notes that the claims do not require that the output driver circuitry of the controller device be configured to a multiplexed bus. The requests notes that the multiplexed bus was an essential element of the original disclosure and the input receiver circuitry must be configured to connected to a multiplexed bus. The request notes since the original disclosure requires a multiplex bus and the instant patent is alleged to not require the multiplex bus, then the '195 patent is not supported by the original disclosure of the '580 parent patent. The request notes that in section 2163.05(I) of the MPEP "under certain circumstances, omission of a limitation can raise an issue regarding whether the inventor had possession of a broader, more generic invention", and "a claim that omits an element which the applicant describes as an essential or critical feature of the invention originally discloses does not comply with the written description requirement.' See pages 11-17 for additional comments, with respect to the "multiplexed bus" made by the requester, which is hereby incorporated by reference.

The request on page 17, notes that the '580 parent patent does not provide support for "transmitting access time information in any way other than as parameters of a packet on a multiplexed bus". See page 17 for comments, with respect to the "transmitting access time information" limitation made by the requester, which is hereby incorporated by reference.

The request on page 17-18, notes that the '580 parent patent does not support claims 1-40 if they do not require two external clock signals. See pages 17-18 for comments, with respect to the "requirement of two external clock signals" limitation made by the requester, which is hereby incorporated by reference.

The request on page 18-19, notes that the '580 parent patent does not support a delay locked loop as required by claims 4,9,14 and 19. See pages 18-19 for comments, with respect to the "delay locked loop" limitation made by the requester, which is hereby incorporated by reference.

Based on this issue, a question is raised as to whether or not the claims are supported by the '580 parent patent, thus the references that predate the filing date of this instant patent, for the purpose of this proceeding as it currently stands, raises a SNQ over the claims of the instant Patent.

Prosecution History

During the prosecution of the 09/196,199 application, the Applicant, in response to the office action mailed on May 27, 1999, file a response on July 1, 1999, which included a terminal disclaimer to obviate the double patenting rejection made by the Examiner. The application was subsequently allowed on July 22, 1999. Supplemental Notice of Allowances were mailed on August 9, 1999 and December 22, 1999 in order to respond to an IDS and other issues. No reasons for allowance were set forth by the Examiner.

Discussion of References that Raise a SNQ

The JEDEC Standard

The request alleges that a SNQ is raised by the **JEDEC Standard** reference.

The JEDEC Standard defines interface design parameters for a Synchronous Dynamic Random Access Memory (SDRAM). Burst length information is received by the SDRAM as part of "mode-of-operation" data that "is written after power-on and before normal operation" to a "Mode Register" located on the SDRAM chip.

The Mode Register Set cycle is initiated by holding the S/, RE/, CE/, and W/signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register.

The JEDEC Standard describes a "Mode Register" that is located on the synchronous DRAM chip. Different values of LTMODE (Latency Mode) set the CE Latency value to different values, which is stored in the Mode Register, (page 3.11.5-8). Address bits 6:4 of the mode-of-operation data contain the Latency Mode information specifying the CAS latency. The CAS latency value indicates when, with respect to the receipt of a read command, the memory device should make data available on the data bus.

See also claim chart exhibit K of the request.

The teaching of a register which stores a value which is representative of a delay time after which the memory device responses to a read request and a plurality of output drivers to output data after the delay time transpires was not discussed on the record during the prosecution of the application which became the '195 patent. Therefore, it is agreed that JEDEC standard, when considered in this new light, raises a SNQ over at least claims 1-24, 27 and 35-37 of the instant '195 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. As discussed above, the priority date of the instant patent is in question and as such the JEDEC Standard reference presents a date of filing or publication which may predate the instant filing date. Accordingly the JEDEC Standard reference raises a SNQ as to at least claims 1-24, 27 and 35-37 of the instant '195 Patent.

Park

The request alleges that a SNQ is raised by the **Park** reference.

For example, as provided in detail via claim chart exhibit L of the request, Park teaches a synchronous dynamic random access memory (abstract), which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU).

Park teaches that the/CAS latency is stored in a register by an operation mode set circuit 58, (col. 13, lines 11-17). The CAS latency value is stored in Address Code Register 202. Park shows in Fig. 13 that the operation mode set circuit 58 includes an "ADDRESS CODE REGISTER" 202 for storing the binary values from address inputs RA0-RA6. Specifically, an operation mode set circuit 58 is responsive to the operation mode set command, so as to set various operation modes, for example, operation modes for establishing a /CAS latency, a burst length representing the number of continuous output data, (col. 13, lines 11-17). Fig. 13 also shows the CAS latency value on the address pins is stored in the Address Code Register 202 in response to the operation mode set command. The operation mode set command is set by the detection of/RAS, /CAS, and/WE low at the clock edge, (col. 12, lines 22-24).

Park states that each delay circuit 500 includes a shift register 504 having a plurality of data paths and switches 497,501, and 402 respectively connected to the data paths, and serves to provide a different time delay via a selected switch according to/CAS latency signals CL3 and CL4, (col. 35, lines 18-22).

See also claim chart exhibit L of the request.

The teaching of a register which stores a value which is representative of a delay time after which the memory device responses to a read request and a plurality of output drivers to output data after the delay time transpires was not present in the prosecution of the application which became the '195 patent and thus it is agreed that Park raises an SNQ over at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. As discussed above, the priority date of the instant patent is in question and as such the Park reference presents a date of filing or publication which may predate the instant filing date. Accordingly, the Park reference raises a SNQ as to at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

The iAPX Manual

The request alleges that a SNQ is raised by the **iAPX Manual.**

It is agreed that the iAPX Manual raises an SNQ over at least claims 1-24, 27 and 32-37 of the '195 Patent.

The iAPX Manual describes during an initialization cycle, the MCU receives a values, that indicates a number of clock cycles to transpire before responding to a read request. The MCU includes an INIT input for starting an initialization cycle, (pages 5-21). The initialization data is loaded from the memory bus and the ACD or SLAD bus while the INIT signal is asserted, (pages 9-1).

The iAPX Manual discloses in the second phase of the initialization (D2) the "s" (Array Speed) parameter is acquired from the SLAD bus and loaded in bit 8 of MCU register 01.

Initial data is received into a buffer, which is connected to the SLAD bus and receive the INIT# signal. "The s field indicates the characteristics that the MCU is to use when accessing the external memory array. The s field indicates whether the MCU will access the storage array with nominal (c-l) or extended (c-0) access time. Extended access time lengthens the nominal access time by one component clock cycle, (pages C-8).

See also claim chart exhibit M of the request.

The teaching of a register which stores a value which is representative of a delay time after which the memory device responses to a read request and a plurality of output drivers to output data after the delay time transpires was not present in the prosecution of the application which became the '195 patent and thus it is agreed that iAPX Manual raises an SNQ over at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Accordingly the iAPX Manual raises a SNQ as to at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

Budde

The request alleges that a SNQ is raised by US Patent 4,480,307 to **Budde et al**.

Budde describes a value called "memory access time in clock cycles" is received into a register at an initialization ("INIT") time. The value represents a number of clock cycles to transpire before the memory device responds to a read request, (col. 10, lines 66 - col. 11, line 6).

Budde discloses memory read data is received by the MCU on the SLAD bus in two cycles, and follows the outgoing address by a specified number of clock cycles. The number of clocks to wait is specified at "INIT .... time as the memory access time, (col. 10, lines 47-51).

In response to a Memory Read Request, the memory device outputs read data in the form of a Read Reply onto the MACD bus. The data from the memory module will be delayed by the memory access time value stored during initialization. Memory read data is received by the MCU on the SLAD bus in two clock cycles, and follows the outgoing address by a specified number of clock cycles. The number of clocks to wait is specified at "INIT" time as the memory access time, (col. 10, lines 47-52).

See also claim chart exhibit N of the request.

The teaching of providing a register which stores a value which is representative of a delay time after which the memory device responses to a read request and a plurality of output drivers to output data after the delay time transpires was not present in the prosecution of the application which became the '195 patent and thus it is agreed that Budde raises an SNQ over at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Accordingly the Budde reference raises a SNQ as to at least claims 1-24, 27 and 32-37 of the instant '195 Patent.

Scope of Reexamination

5. Since requester did not request reexamination of claims 25, 26, 28-31 and 38-40 and did not assert the existence of a substantial new question of patentability (SNQP) for such claims

(see 35 U.S.C. § 311(b)(2); see also 37 CFR 1.915b and 1.923), such claims will not be reexamined. This matter was squarely addressed in *Sony Computer Entertainment America Inc., et al. v. Jon W. Dudas*, Civil Action No. 1:05CV1447 (E.D.Va. May 22, 2006), Slip Copy, 2006 WL 1472462. (Not Reported in F.Supp.2d.) The District Court upheld the Office's discretion to not reexamine claims in an *inter parte* reexamination proceeding other than those claims for which reexamination had specifically been requested. The Court stated:

> To be sure, a party may seek, and the PTO may grant, *inter partes* review of each and every claim of a patent. Moreover, while the PTO in its discretion may review claims for which *inter partes* review was not requested, nothing in the statute compels it to do so. To ensure that the PTO considers a claim for *inter partes* review, § 311(b)(2) requires that the party seeking reexamination demonstrate why the PTO should reexamine each and every claim for which it seeks review. Here, it is undisputed that Sony did not seek review of every claim under the '213 and '333 patents. Accordingly, Sony cannot now claim that the PTO wrongly failed to reexamine claims for which Sony never requested review, and its argument that AIPA compels a contrary result is unpersuasive.

The *Sony* decision's reasoning and statutory interpretation apply analogously to *ex parte* reexamination, as the same relevant statutory language applies to both *inter partes* and *ex parte* reexamination. 35 U.S.C. § 302 provides that the *ex parte* reexamination "request must set forth the pertinency and manner of applying cited prior art to every claim for which reexamination is requested" (emphasis added), and 35 U.S.C. § 303 provides that "the Director will determine whether a substantial new question of patentability affecting any claim of the patent concerned is raised by the request..." (Emphasis added). These provisions are analogous to the language of 35 U.S.C. § 311(b)(2) and 35 U.S.C. § 312 applied and construed in *Sony*, and would be construed in the same manner. As the Director can decline to reexamine non-requested claims in an *inter parte* reexamination proceeding, the Director can likewise do so in *ex parte*

reexamination proceeding. See *Notice of Clarification of Office Policy To Exercise Discretion in Reexamining Fewer Than All the Patent Claims* (signed Oct. 5, 2006) 1311 OG 197 (Oct. 31, 2006). See also MPEP § 2240, Rev. 5, Aug. 2006.

Therefore, claims 25, 26, 28-31 and 38-40 will not be reexamined in this *ex parte* reexamination proceeding.

6. Claims 1-24, 27 and 32-37 will be reexamined as requested in the request.

Conclusion

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

7. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

8. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,038,195 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

9. All correspondence related to this *ex parte* reexamination proceeding should be directed as follows:

Please MAIL any communications to:

Attn: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Please FAX any communication to:

(571) 273-9900
Central Reexamination Unit

Please HAND-DELIVER any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

10. Any inquiry by the patent owner concerning this communication or earlier communications from the Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Ovidio Escalante

Ovidio Escalante
Primary Examiner
Central Reexamination Unit - Art Unit 3992
(571) 272-7537

Conferee:

PRIMARY EXAMINER
CRU 3992

Conferee:

MARK J. REINHART
CRU SPE-AU 3992

PTO/SB/08a (05-07)
Approved for use through 09/30/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2007-12-17
	First Named Inventor	Farmwald et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	38512.11

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
OE	1	5590086		1996-12-31	Park et al.	
OE	2	4480307		1984-10-30	Budde et al.	
OE	3	5361277		1994-11-01	Grover	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
OE	1	2197553	GB		1988-05-18	Lofgren et al.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2007-12-17
	First Named Inventor	Farmwald et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	38512.11

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
OE	1	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Release 4, November 1993.	☐
OE	2	Intel Corporation, "iAPX 432 Interconnect Architecture Reference Manual", published in 1982.	☐
OE	3	Intel Corporation, "Electrical Specifications for iAPX 43204 Bus-Interface unit (BIU) and iAPX 43205 Memory Control Unit (MCU)", published March 1983.	☐
OE	4	Johnson et al., "A Variable Delay Line PLL for CPU - Coprocessor Synchronization", IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, published October 1988.	☐
OE	5	Rau et al., "The Cydra 5 Departmental Supercomputer Design Philosphies, Decisions, and Tradeoffs", published January 1989.	☐

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