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CONTROL NO.	FILING DATE	PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
95/001,013	10/11/07	6,697,295	

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EXAMINER
ALBERT PALADINI

ART UNIT	PAPER
3992	

DATE MAILED:

01/09/08

INTER PARTES REEXAMINATION COMMUNICATION

BELOW/ATTACHED YOU WILL FIND A COMMUNICATION FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE OFFICIAL(S) IN CHARGE OF THE PRESENT REEXAMINATION PROCEEDING.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this communication.

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Date:

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. : 95001013
PATENT NO. : 6697295
ART UNIT : 3900

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified ex parte reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the ex parte reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Transmittal of Communication to Third Party Requester Inter Partes Reexamination	Control No.	Patent Under Reexamination	
	95/001,013	6697295	
	Examiner	Art Unit	
	Albert W. Paladini	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

ORDER GRANTING/DENYING REQUEST FOR* INTER PARTES *REEXAMINATION	**Control No.**	**Patent Under Reexamination**	
	95/001,013	6697295	
	Examiner	**Art Unit**	
	Albert W. Paladini	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

The request for *inter partes* reexamination has been considered. Identification of the claims, the references relied on, and the rationale supporting the determination are attached.

Attachment(s): ☐ PTO-892 ☒ PTO/SB/08 ☐ Other: _____

1. ☒ The request for *inter partes* reexamination is GRANTED.

   ☐ An Office action is attached with this order.

   ☒ An Office action will follow in due course.

2. ☐ The request for *inter partes* reexamination is DENIED.

This decision is not appealable. 35 U.S.C. 312(c). Requester may seek review of a denial by petition to the Director of the USPTO within ONE MONTH from the mailing date hereof. 37 CFR 1.927. EXTENSIONS OF TIME ONLY UNDER 37 CFR 1.183. In due course, a refund under 37 CFR 1.26(c) will be made to requester.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Order.

DECISION GRANTING *INTER PARTES* REEXAMINATION

A substantial new question of patentability affecting claims 1-51 of United States Patent Number 6,697,295 (issued to Farmwald et al.) is raised by the present request for *inter partes* reexamination.

An Office action on the merits does not accompany this order for *inter partes* reexamination. An Office action on the merits will be provided in due course.

References Cited in the Request

Page 6 of the Request identifies the following printed publications as providing teachings relevant to the claims of the '295 Farmwald patent

Exhibit B	Joint Electron Device Engineering Council (**JEDEC**) Standard No. 21-C, Revision 9 **published in 1999** (the JEDEC Standard).
Exhibit C	U.S. Patent No. 5,590,086 to Park et al. (**Park**) issued on **December 31, 1996**.
Exhibit D, Tab 1	Intel Corporation iAPX 432 Interconnect Architecture Reference Manual, **published 1982** (the **iAPX Manual**).
Exhibit D, Tab 2	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), **published March 1983** (the **iAPX Specification**).
Exhibit E Tab 1	US Patent 4,480,307 to Budde et al. (**Budde**) issued **October 30, 1984**.
Exhibit E Tab 2	US Patent 4,438,494 to Budde et al. (**Budde-II**) issued **March 20, 1984**.
Exhibit F	Inagaki, Japanese Patent JP 57-210495 to NEC Corp. published **December 24, 1982** (**Inagaki**).
Exhibit G	US Patent 5,361,277 to **Grover**, issued **November 1, 1994** (Grover).

Exhibit H	UK Published Patent App. No. GB 2197553 to Lofgren et al. **published May 18, 1988 (Lofgren)**.
Exhibit I	Johnson et al., A Variable Delay Line PLL for CPU - Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, **published October 1988 (Johnson)**.
Exhibit J	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Tradeoffs, **published in January 1989 (Rau)**

Detailed Explanation of How the Cited Prior Art is Applied to Every Claim for Which Reexamination is Requested.

Alleged Anticipatory SNQs Based on Intervening References

Issue 1: The JEDEC Standard is asserted as rendering claims 1,8, 16-18, 31, 32, and 43-45 anticipated.

Issue 2: US Patent 5,590,086 to Park et al. is asserted as rendering claims 1, 8, 16-18, 31, and 32 anticipated

Alleged Anticipatory SNQs based on Prior Art

Issue 3: iAPX Manual is asserted as rendering claims 1, 4-11, 13, 14, 16-22, 25, 27-33, 38-40, and 46-51 anticipated.

Issue 4: US Patent 4,480,307 to Budde et al. is asserted as rendering claims 1, 4-11, 13, 14, 16-22, 25, 27-33, 38-40, and 46-51 anticipated.

Alleged Obviousness SNQs Based on Intervening References

Issue 5: Park in view of the JEDEC Standard is asserted as rendering claims 43 and 44 obvious.

Issue 6: Park in view of Grover is asserted as rendering claims 43 and 44 obvious.

Issue 7: Park in view of Lofgren is asserted as rendering claims 43 and 44 obvious.

Issue 8: Park in view of Johnson is asserted as rendering claims 43 and 44 obvious.

Issue 9: Park in view of Inagaki and Johnson is asserted as rendering claim 45 obvious.

Alleged Obviousness SNQs based on Prior Art

Issue 10: iAPX Manual in view of iAPX Specification is asserted as rendering claims 1, 4-11, 13, 14, 16-22, 25, 27-33, 38-40, and 46-51 obvious.

Issue 11: iAPX Manual in view of Rau is asserted as rendering claims 2, 3, 23, 24, and 35-37 obvious.

Issue 12: iAPX Manual in view of Grover is asserted as rendering claims 43 and 44 obvious.

Issue 13: iAPX Manual in view of Lofgren is asserted as rendering claims 43 and 44 obvious.

Issue 14: iAPX Manual in view of Johnson is asserted as rendering claims 43 and 44 obvious.

Issue 15: iAPX Manual in view of Inagaki is asserted as rendering claims 12 and 34 obvious.

Issue 16: iAPX Manual in view of Inagaki and Johnson is asserted as rendering claim 45 obvious.

Issue 17: Budde in view of Budde-II is asserted as rendering claims 1, 4-11, 13-22, 25-33, 38-42, and 46-51 obvious.

Issue 18: Budde in view of Rau is asserted as rendering claims 2, 3, 15, 23, 24, 26, 35-37, 41, and 42 obvious.

Issue 19: Budde in view of Grover is asserted as rendering claims 43 and 44 obvious.

Issue 20: Budde in view of Lofgren is asserted as rendering claims 43 and 44 obvious.

Issue 21: Budde in view of Johnson is asserted as rendering claims 43 and 44 obvious.

Issue 22: Budde in view of Inagaki is asserted as rendering claims 12 and 34 obvious.

Issue 23: Budde in view of Inagaki and Johnson is asserted as rendering claim 45 obvious.

Alleged anticipatory issues 1-2 and alleged obviousness issues 5-9 comprise art that fails to antedate the original filing date of a patent Application of which the instant '295 Patent claims benefit. This issue will be discussed *infra*.

Priority Issues Related to Oath or Declaration

The Requester on pages 10-23 of the request asserts that the instant '295 Patent should not be accorded the filing date of the original '898 Patent Application ("the '898 Application"). This is due to Requester's allegation that the parent Patent of the instant '295 Patent failed to present a proper oath or declaration specifically referring to the initial preliminary amendment filed with the initial application.

The issue of whether certain claims of the '295 patent are not entitled to an earlier effective filing date because such claims contain elements that are argued to have been supplied by a preliminary amendment that was not covered by the 37 CFR 1.63 declaration of record will not be decided in this Order. As discussed below, the request is deemed to establish a substantial new question of patentability for the '295 claims on other bases. Therefore, the Office will accept jurisdiction over the '295 on those "more conventional" SNQs. The question raised with respect to lack of entitlement to an earlier effective filing date because the 37 CFR 1.63 declaration filed in the application that matured into the '295 patent did not "cover" the preliminary amendment that added support for certain claim features is reserved for the first Office action on the merits.

Priority Issues Related to the References/Instant Claims

The MPEP states "to be entitled to an earlier priority date or filing date under 35 U.S.C. 119, 120, or 365(c), each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure." MPEP 2163 II.A.3(b).

A rejection may be made in an inter-partes reexamination proceeding based on an intervening patent when the patent claims under reexamination, under 35 U.S.C. 120, are entitled only to the filing date of the patent under reexamination. Specifically:

> Rejections on art in reexamination proceedings may only be made on the basis of prior art patents or printed publications. See MPEP § 2258 and § 2258.01 for a discussion of art rejections in reexamination proceedings based on prior art patents or printed publications.

(MPEP § 2658.1, Scope of Inter Partes Reexamination) (emphasis added).

> Rejections may be made in reexamination proceedings based on intervening patents or printed publications where the patent claims under reexamination are entitled only to the filing date of the patent and are not supported by an earlier foreign or United States patent application whose filing date is claimed. For example, under 35 U.S.C. 120, the effective date of these claims would be the filing date of the application which resulted in the patent. Intervening patents or printed publications are available as prior art under In re Ruscetta, 255 F.2d 687, 118 USPQ 101 (CCPA 1958), and In re van Langenhoven, 458 F.2d 132, 173 USPQ 426 (CCPA 1972). See also MPEP § 201.11

(MPEP § 2258.1.C, Scope of Reexamination) (emphasis added).

To be entitled to priority under 35 U.S.C. 120, the previously filed application of the parent patent must comply with 35 U.S.C. 112, first paragraph. Specifically:

> An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, ms though fled on the date of the prior application[.]

(35 U.S.C. 120, Benefit of Earlier Filing Date in the U.S.)

35 U.S.C. 112, 1st paragraph, in turn, requires the written description of the application describe the claimed invention with sufficient particularity that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. Vas-

Cath Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-17 (Fed. Cir. 1991). See also MPEP § 2163.

Thus, in reexamination, an analysis of the instant Patent's effective priority date is proper.

Analysis

Third Party alleges on pp. 12-23 of the request a number of features in the claims that are allegedly not supported by the original disclosure of the '051 parent patent under 35 U.S.C. §112. The references that predate March 7, 2001, for the purposes of this proceeding as it currently stands thus may potentially raise a SNQ over claims of the instant Patent.

The request notes that the claims do not require that the output driver circuitry of the controller device be configured to a multiplexed bus. The requests notes that the multiplexed bus was an essential element of the original disclosure and the input receiver circuitry must be configured to connected to a multiplexed bus. The request notes since the original disclosure requires a multiplex bus and the instant patent is alleged to not require the multiplex bus, then the '295 patent is not supported by the original disclosure of the '051 parent patent. The request notes that in section 2163.05(I) of the MPEP "under certain circumstances, omission of a limitation can raise an issue regarding whether the inventor had possession of a broader, more generic invention", and "a claim that omits an element which the applicant describes as an essential or critical feature of the invention originally discloses does not comply with the written description requirement.' See pages 12-18 for additional comments, with respect to the "multiplexed bus" made by the requester, which is hereby incorporated by reference.

The request on page 18, notes that the '051 parent patent does not provide support for "transmitting access time information, block size information, and operation codes in any way

other than as parameters of a packet on a multiplexed bus". See pages 18-19 for comments, with respect to the "transmitting access time information, block size information, and operation codes" limitation made by the requester, which is hereby incorporated by reference.

The request on page 20, notes that the '051 parent patent does not support claims if they do not require two external clock signals. See page 20 for comments, with respect to the "requirement of two external clock signals" limitation made by the requester, which is hereby incorporated by reference.

The request on pages 20 and 21, notes that the '051 parent patent does not support sampling data on the transition of an external clock signal. See pages 20 and 21 for comments, with respect to the "sampling data on the transition of an external clock signal" limitation made by the requester, which is hereby incorporated by reference.

The request on pages 21 and 22, notes that the '051 parent patent does not support outputting data and control information on both the rising and falling edge of an external clock signal. See pages 21-22 for comments, with respect to the "outputting data and control information on both the rising and falling edge of an external clock signal" limitation made by the requester, which is hereby incorporated by reference.

The request on page 22, notes that the '051 parent patent does not support a delay locked loop. See page 22 for comments, with respect to the "delay locked loop" limitation made by the requester, which is hereby incorporated by reference.

Based on this issue, a question is raised as to whether or not the claims are supported by the '051 parent patent, thus the references that predate the filing date of this instant patent, for the

purpose of this proceeding as it currently stands, raises a SNQ over the claims of the instant Patent.

Prosecution History

During prosecution of the 09/801,151 application, no prior art rejections were applied to claim 151, which was renumbered to claim 1 in the '295 patent. Independent claims 164 and 173 were rejected under 35 USC 102(b) as being anticipated by Aoyama 4,823,321 in the office action mailed March 13, 2002 (dependent claims 165-172 and 174-192 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form).

The Applicant's response on April 3, 2002 argued that Aoyama does not teach "issuing a first operation code to the memory device, wherein the first operation code initiates an access of a programmable register in order to store a memory value" in claims 164 and 173. Applicant also amended claims 164 and 173 to include the limitation that the binary value "is representative of control information". Claims 164 and 173 were renumbered as independent claims 16 and 31 at allowance.

Discussion of References that Raise a SNQ

Issue 1

The request alleges that a SNQ is raised by the **JEDEC Standard** reference.

The JEDEC Standard reference was cited during prosecution of the Farmwald et al. patent, but was not applied during prosecution in a rejection of a claim. Thus, a substantial new question

of patentability would facially be based on patents and/or printed publications already cited/considered in an earlier concluded examination of the patent being reexamined. However, on November 2, 2002, Public Law 107-273 was enacted. Title III, Subtitle A, Section 13105, part (a) of the Act revised the reexamination statute by adding the following new last sentence to 35 U.S.C. 303(a) and 312(a):

> "The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office."

For any reexamination ordered on or after November 2, 2002, the effective date of the statutory revision, reliance on previously cited/considered art, i.e., "old art," does not necessarily preclude the existence of a substantial new question of patentability (SNQ) that is based exclusively on that old art. Rather, determinations on whether a SNQ exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis.

A discussion of the specifics now follows:

Requestor discusses the limitation of sampling a first operation code synchronously with respect to a transition of an external clock signal, and alleges that the CAS latency value in the JEDEC standard is the first operation code. The sampling process is described in the JEDEC standard in sections 3.11.5.1.3 and 3.11.5.1.7 where a CAS latency value is received by the SDRAM as part of mode operations data. The transition is described in section 3.11.5.1.7 of the JEDEC standard which states "The Mode Set Register Set Cycle is initiated by holding the /S, /RE, /CE and /W signals low at the clock rising edge."

Requestor discusses the limitation of receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, and explains that the JEDEC standard alleges the CAS value received as part of the mode of operation data written to a Mode Register Is equivalent to the binary value as described in section 3.11.5.1.3 of the JEDEC standard. The Requestor alleges that the second operation code recited by Farmwald is equivalent to a read command discussed in section 3.11.5.1.6 of the JEDEC standard, where control signals /S, /RE, /CE and /W are used to instruct toe memory device to perform a read operation, as shown in Table 3.11.5.1-1 of the JEDEC manual. The Requestor explains that this table also demonstrates that "The CAS latency value indicates when, with respect to the receipt of a red command, the memory device should make data available on the bus".

Requestor discusses the limitation of wherein the second operation code specifies a read operation to the memory device, and explains that control signals /S, /RE, /CE and /W described in table 3.11.5.1.16 of the JEDEC manual , which instruct the memory to perform read and write operations are allegedly equivalent to the second operation code recited by Farmwald.

Requestor discusses the limitation of storing the binary value in the programmable register in response to the first operation code, and explains that "The CAS latency value is stored in the mode register in response to the mode set register command" as described in section 3.11.5.1.7 is allegedly equivalent to Farmwald's limitation.

On pages 5-7, the Requestor enumerates all recited elements of representative independent claims 16 and 31 of Farmwald, and suggests corresponding elements discussed in reference JEDEC standard. See the claim chart exhibit K of the request.

At least the teaching in the JEDEC standard of the binary value being representative of control information, or more specifically, representative of a delay time to transpire before the memory device is to output data in response to a second operation code was not considered or discussed on the record during the prosecution of the application which became the '295 patent. Therefore, it is agreed that JEDEC standard, when considered in this new light, raises a SNQ over at least claims 1, 16, and 31 of the instant '295 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. As discussed above, the priority date of the instant patent is in question and as such the JEDEC Standard reference presents a date of filing or publication which may predate the instant filing date. Accordingly the JEDEC Standard reference raises a SNQ as to at least claims 1, 16, and 31 of the instant '295 Patent.

Issues 2 and 5-9

The request alleges that several SNQs are raised by the **Park** reference.

For example, as provided in detail via claim chart exhibit L, the Requestor enumerates all recited elements of representative independent claim 1 of Farmwald, and suggests corresponding elements discussed in reference Park.

On page 1, the Requestor discusses Farmwald's limitation of sampling a first operation code synchronously with respect to a transition of an external clock signal, and alleges that the operation mode set command is equivalent to the first operation code discussed by Park. Referring to Park. The Requestor states "Fig. 20 shows that the operation mode set command is applied at time t1, which corresponds to the rising edge of the external clock CLK. Col 10, lines 1-4"

On pages 2 and 3, the Requestor discusses Farmwald's limitation of receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, and alleges that the /CAS latency signal taught by Park is equivalent to the binary value. With respect to the external clock signal, Park states in (C12, L21-24) "An establishment of operation mode set command according to a feature of the present invention is accomplished at low levels of RAS, CAS and WE at the leading edge of the clock CLK". With respect to the binary value, Park states in (C18, L15-32) "A latency logic circuit 206 produces a /CAS latency signal CL_j generated with logic combinations of the codes MDST4 to MDST6". With respect to the delay time, Park states in (C18, L60-64) " It will be noted that the values of /CAS latency j in the above tables represents the number of system and /CAS latency values related to maximum clock values may be changed according to a synchronous RAM. With respect to synchronously receiving a binary code, the Requestor states on page 3 "See also Fig. 13, Table 1, Col 18. Fig 20 shows that the operation mode set command is applied at time t1, which corresponds to the rising edge of the external clock CLK, Col 19, lines 10-14."

On page 3, the Requestor discusses Farmwald's limitation of wherein the second operation code specifies a read operation to the memory device, and alleges the read operation in the statement "Commands such as the read command are sent by using control signals (e.g., /RAS, /CAS, /WE and /CS S)" Park states in (C12, L13-15) "After the activation, at the leading edge of the system clock CLK, the high level /RAS, the low level /CAS, and the high level /WE indicate a read command".

On pages 3 and 4, the Requestor discusses Farmwald's limitation of storing the binary value in the programmable register in response to the first operation code, and alleges that this is equivalent to Park storing the /CAS latency in a register by operation mode set circuit 58 as described by Park in (C13, L11-17).

The Requestor enumerates all recited elements of representative independent claims 16 and 31 of Farmwald, and suggests corresponding elements discussed in Park. See the claim chart exhibit L of the request.

At least the teaching in Park of the binary value being representative of control information, or more specifically, representative of a delay time to transpire before the memory device is to output data in response to a second operation code was not considered or discussed on the record during the prosecution of the application which became the '295 patent. Therefore, it is agreed that Park raises a SNQ over at least claims 1, 16, and 31 of the instant '295 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. As discussed above, the priority date of the instant patent is in question and as such the Park reference presents a date of filing or publication which may

predate the instant filing date. Accordingly the Park reference raises a SNQ as to at least claims 1, 16, and 31 of the instant '295 Patent.

Issues 3 and 10-16

The request alleges that several SNQs are raised by the **iAPX Manual.**

It is agreed that the iAPX Manual raises an SNQ over at least claims 1-14, 16-25, 27-40, and 43-51 of the '295 Patent.

On pages 1-4 of Exhibit M, the Requestor enumerates all recited elements of representative independent claim 1 of Farmwald, and suggests corresponding elements discussed in reference iAPX.

On pages 1 and 2, the Requestor discusses Farmwald's limitation of sampling a first operation code synchronously with respect to a transition of an external clock signal, and states "The iAPX Manual generally describes that the processors (including the MCU) are kept in 'lock step' by operating with respect to a transition (clock edge) of an external clock Pg. 4-15. More specifically, the iAP specification (Exhibit D, Tab 2) shows that the INIT input is sampled synchronously with respect to the rising edge of the external clock CLKA, Pg. MCU-36."

On pages 2 and 3, the Requestor discusses Farmwald's limitation of receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, and describes the alleged equivalency described by the iAPX manual in the statement "During an initialization cycle, the MCU receives a value 's', which indicates a number of clock cycles to transpire before responding to a read request." The Requestor states on

page 3 "The MACD bus is synchronous, and includes two clock signals –CLKA and CLKB. Since it is synchronous, the values provided over the bus are synchronous."

On pages 3 and 4, the Requestor discusses Farmwald's limitation of wherein the second operation code specifies a read operation to the memory device, and describes the alleged equivalent read operation of iAPX in the statement "The MCU is a synchronous device that communicates over the memory (MACD) bus using message packets, including a Memory Read Request message. Pgs. F2, F5. 'The memory requests are issued to a memory bus as packets of information.' The BIU sends requests to the MCU. See 1-4. 1-4. Fig. 1-2".

On page 4, the Requestor discusses Farmwald's limitation of storing the binary value in the programmable register in response to the first operation code, and suggests that the iAPX manual performs the equivalent function in the statement "The 's field is a field of MCU register 01, called the 'Interconnect Device Type" register, which is a control register. Pg. C-7. The 's' parameter is written into the Interconnect Device Type register during initialization, which is started by assertion of the INIT signal. Pg 9-7.

See also claim chart exhibit M of the request.

At least the teaching in the iAPX Manual of the binary value being representative of control information, or more specifically, representative of a delay time to transpire before the memory device is to output data in response to a second operation code was not considered or discussed on the record during the prosecution of the application which became the '295 patent. Other issues alleged by the Requester, such as Issues 10-16, raises a SNQ for the same reasoning set forth above with respect to issue 3. Therefore, it is agreed that the iAPX Manual raises a SNQ over at least claims 1-14, 16-25, 27-40, and 43-51 of the instant '295 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Furthermore, the iAPX Manual was not before the examiner during the prosecution of the '295 patent. Accordingly the iAPX Manual raises a SNQ as to at least claims 1-14, 16-25, 27-40, and 43-51 of the instant '295 Patent.

Issues 4 and 17-23

The request alleges that several SNQs are raised by US Patent 4,480,307 to **Budde et al**.

(2) On pages 1-4 of Exhibit N, the Requestor enumerates all recited elements of representative independent claim 1 of Farmwald, and alleges corresponding elements discussed in reference Budde.

On pages 1 and 2, the Requestor discusses Farmwald's limitation of sampling a first operation code synchronously with respect to a transition of an external clock signal, and suggests that Budde teaches sampling the first operation code in the statement "The MCU receives a plurality of control signals, one of which is the INIT signal line which transmits an INIT# signal that starts an initialization and configuration and reset operation. Col.7, lines 5-10, 20-23." The Requestor suggests that Budd teaches the synchronicity and the relation to the clock signal in the statement "Budd teaches clock signals CLKA and CLKB for use in the synchronous operation of the MACD bus. Col. 7, Lines 11-19".

On pages 2 and 3, the Requestor discusses Farmwald's limitation of receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response

to a second operation code, and suggests that Budde teaches the received binary value in the statement "A value called 'memory access time in clock cycles' is included with the initialization and configuration information provided during the Init cycle. The value represents a number of clock cycles to transpire before the memory device responds to a read request. Col. 10, line 66 – Col 11. line 6." The Requestor suggests that Budde teaches the memory device outputting data in response to a second operation code in the statement "Memory read data is received by the MCU on the SLAS bus in two clock cycles, and follows the outgoing addresses by a specified number of clock cycles. The number of clocks to wait is specified at 'INIT' time as the memory access time.' Col. 10, lines 47-52."

On pages 3 and 4, the Requestor discusses Farmwald's limitation of wherein the second operation code specifies a read operation to the memory device, and suggests that Budde teaches the read operation in the statement "Read requests are received by the memory device on the MACD bus within a packet and sampled with respect to a transition of external clock signal CLKB. The memory Read Request is sent from the BIU. Col 12, lines 44-45."

On page 4, the Requestor discusses Farmwald's limitation of storing the binary value in the programmable register in response to the first operation code, and suggests that Budde teaches storing the binary value in the statement "The parameters provided during the INIT time are stored by the MCU because they can only be provided during INIT, but are used at a later time. Col. 10, lines 47-51 provides an example of where the access time was set to 2 cycles during the INIT time, and cannot be changed unless another INIT time is initiated."

See also claim chart exhibit M of the request.

At least the teaching in Budde of the binary value being representative of control information, or more specifically, representative of a delay time to transpire before the memory device is to output data in response to a second operation code was not considered or discussed on the record during the prosecution of the application which became the '295 patent. Other issues alleged by the Requester, such as Issues 17-23, raises a SNQ for the same reasoning set forth above with respect to issue 5. Therefore, it is agreed that Budde raises a SNQ over at least claims 1-51 of the instant '295 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Furthermore, Budde was not before the examiner during the prosecution of the '295 patent. Accordingly Budde raises a SNQ as to at least claims 1-51 of the instant '295 Patent.

Scope of Reexamination

All of claims 1-51 will be reexamined as requested in the request.

Conclusion

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes* reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c) requires that inter partes reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.937). Patent owner extensions of time in inter partes reexamination proceedings are provided for in 37 CFR 1.956. Extensions of time are not available for third party requester comments, because a comment period of 30 days from service of patent owner's response is set by statute. 35 U.S.C. 314(b)(3).

The Patent Owner is reminded of the continuing responsibility under 37 CFR 1.985(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the US Patent 6,697,295 throughout the course of this reexamination proceeding. The Third Party Requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding through the course of this reexamination proceeding. See MPEP § 2686 and 2686.04.

All correspondence relating to this *inter partes* reexamination proceeding should be directed as follows:

By **U.S. Postal Service Mail** to:

Mail Stop *Inter Partes* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building
401 Dulany St.
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

Albert W. Paladini
Primary Examiner

Conferees:

ESK

Ovidio Escalante