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RAMBUS INC.
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EXAMINER	
ESCALANTE, OVIDIO	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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CENTRAL REEXAMINATION UNIT

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

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Transmittal of Communication to Third Party Requester
Inter Partes Reexamination

REEXAMINATION CONTROL NUMBER *95/001,026*.

PATENT NUMBER *6,378,020*.

TECHNOLOGY CENTER *3900*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

ORDER GRANTING/DENYING REQUEST FOR* INTER PARTES *REEXAMINATION	**Control No.**	**Patent Under Reexamination**	
	95/001,026	6378020	
	Examiner	**Art Unit**	
	OVIDIO ESCALANTE	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

The request for *inter partes* reexamination has been considered. Identification of the claims, the references relied on, and the rationale supporting the determination are attached.

Attachment(s): ☐ PTO-892 ☒ PTO/SB/08 ☒Other: Decision

1. ☒ The request for *inter partes* reexamination is GRANTED.

   ☐ An Office action is attached with this order.

   ☒ An Office action will follow in due course.

2. ☐ The request for *inter partes* reexamination is DENIED.

This decision is not appealable. 35 U.S.C. 312(c). Requester may seek review of a denial by petition to the Director of the USPTO within ONE MONTH from the mailing date hereof. 37 CFR 1.927. EXTENSIONS OF TIME ONLY UNDER 37 CFR 1.183. In due course, a refund under 37 CFR 1.26(c) will be made to requester.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Order.

DECISION GRANTING *INTER PARTES* REEXAMINATION

1. A substantial new question of patentability affecting claims 30-33,35-36 and 38-41 of United States Patent Number 6,378,020 (Farmwald et al. patent) is raised by the request for *inter partes* reexamination.

An Office action on the merits does not accompany this order for *inter partes* reexamination. An Office action on the merits will be provided in due course.

2. The instant patent issued April 23, 2002 based on US Patent Application Ser. No. 09/545,648, filed April 10, 2000 as a continuation of U.S. Patent 09/161,090, filed September 25, 1998, now U.S. Patent 6,049,846 as a division of U.S. application 08/798,520, filed February 10, 1997, now U.S. Patent 5,841,580 as a division of U.S. application 08/448,657, filed May 24, 1995, now U.S. Patent 5,638,334, as a division of U.S. application 08/222,646, filed on March 31, 1994, now U.S. Patent 5,513,327 as a continuation of U.S. application 07/954,954, filed September 30, 1992, now U.S. Patent 5,319,755 as a continuation of U.S. Application 07/510,898, filed April 18, 1990.

References Cited in the Request

3. Page 6 of the Request identifies the following printed publications as providing teachings relevant to the claims of the '8,020 Farmwald patent

Exhibit B	Joint Electron Device Engineering Council (**JEDEC**) Standard No. 21-C, Revision 9 **published in 1999 (the JEDEC Standard).**
Exhibit C	Hyundai, HY5DV651622, Rev. 0.9, **published January 2000 (Hynix-1).**
Exhibit D	Inagaki, Japanese Patent JP 57-210495 to NEC Corp. **published December 24, 1982 (Inagaki).**

Exhibit E	US Patent 5,361,277 to **Grover**, issued **November 1, 1994** (Grover).
Exhibit F	U.S. Patent No. 5,590,086 to Park et al. (**Park**) **issued on December 31, 1996**.
Exhibit G, Tab 1	Intel Corporation iAPX 432 Interconnect Architecture Reference Manual, **published 1982 (the iAPX Manual)**.
Exhibit G, Tab 2	Intel Corporation, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 memory control unit (MCU), **published March 1983 (the iAPX Specification)**.
Exhibit H	US Patent 4,480,307 to Budde et al. (**Budde**) **issued October 30, 1984**.
Exhibit I	Intel Corporation, Memory Components Handbook, Chapter 1 and Chapter 3, **published 1982 and 1985 (the iRAM reference).**

Detailed Explanation of How the Cited Prior Art is Applied to Every Claim for Which Reexamination is Requested.

Alleged Anticipatory SNQs Based on Intervening Art

Issue 1: The JEDEC Standard is asserted as rendering claims 30-33, 35-36 and 38-41 anticipated.

Issue 2: The Hynix-1 reference is asserted as rendering claims 30-32, 35-36 and 38 anticipated.

Alleged Obviousness SNQs Based on Intervening Art

Issue 3: Park in view of the JEDEC Standard is asserted as rendering claims 30-33, 35-36 and 38 obvious.

Alleged Obviousness SNQs based on Prior Art

Issue 4 iAPX Manual in view of Inagaki is asserted as rendering claims 30-33 and 38-41 obvious.

Issue 5: iAPX Manual in view of iAPX Specification is asserted as rendering claims 30-33 and 38-41 obvious

Issue 6: iAPX Manual in view of Inagaki and Grover is asserted as rendering claims 35-36 obvious.

Issue 7: Budde in view of Inagaki is asserted as rendering claims 30-33 and 38-41 obvious.

Issue 8: Budde in view of Inagaki and Grover is asserted as rendering claims 35-36 obvious.

Issue 9: iAPX Manual in view of Inagaki and the iRAM reference is asserted as rendering claims 30-33 and 38-41 obvious.

Issue 10: iAPX Manual in view of Inagaki, Grover and the iRAM reference is asserted as rendering claims 35-36 obvious.

Issue 11: Budde in view of Inagaki and the iRAM reference is asserted as rendering claims 30-33 and 38-41 obvious.

Issue 12: Budde in view of Inagaki and Grover and the iRAM reference is asserted as rendering claims 35-36 obvious.

Alleged anticipatory issues 1-2 and alleged obviousness issue 3 comprise art that fails to antedate the original filing date of a patent Application of which the instant '8,020 Patent claims benefit. This issue will be discussed *infra*.

Priority Issues Related to Oath or Declaration

The Requester on pages 9-10 of the request asserts that the instant '8,020 Patent should not be accorded the filing date of the original '846 Parent Patent ("the '846 Patent"). This is due to Requester's allegation that the parent Patent of the instant '8,020 Patent failed to present a proper oath or declaration specifically referring to the initial preliminary amendment filed with the initial application.

The issue of whether certain claims of the '8,020 patent are not entitled to an earlier effective filing date because such claims contain elements that are argued to have been supplied by a preliminary amendment that was not covered by the 37 CFR 1.63 declaration of record will not be decided in this Order. As discussed below, the request is deemed to establish a substantial new question of patentability for the '8,020 claims on other bases. Therefore, the Office will accept jurisdiction over the '8,020 on those "more conventional" SNQs. The question raised with respect to lack of entitlement to an earlier effective filing date because the 37 CFR 1.63 declaration filed in the application that matured into the '8,020 patent did not "cover" the preliminary amendment that added support for certain claim features is reserved for the first Office action on the merits.

Priority Issues Related to the References/Instant Claims

The MPEP states "to be entitled to an earlier priority date or filing date under 35 U.S.C. 119, 120, or 365(c), each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure." MPEP 2163 II.A.3(b).

> A rejection may be made in an inter-partes reexamination proceeding based on an intervening patent when the patent claims under reexamination, under 35 U.S.C. 120, are entitled only to the filing date of the patent under reexamination. Specifically:
>
> > Rejections on art in reexamination proceedings may only be made on the basis of prior art patents or printed publications. See MPEP § 2258 and § 2258.01 for a discussion of art rejections in reexamination proceedings based on prior art patents or printed publications.

(MPEP § 2658.1, Scope of Inter Partes Reexamination) (emphasis added).

> Rejections may be made in reexamination proceedings based on intervening patents or printed publications where the patent claims under reexamination are entitled only to the filing date of the patent and are not supported by an earlier foreign or United States patent application whose filing date is claimed. For example, under 35 U.S.C. 120, the effective date of these claims would be the filing date of the application which resulted in the patent. Intervening patents or printed publications are available as prior art under In re Ruscetta, 255 F.2d 687, 118 USPQ 101 (CCPA 1958), and In re van Langenhoven, 458 F.2d 132, 173 USPQ 426 (CCPA 1972). See also MPEP § 201.11

(MPEP § 2258.1.C, Scope of Reexamination) (emphasis added).
To be entitled to priority under 35 U.S.C. 120, the previously filed application of the parent patent must comply with 35 U.S.C. 112, first paragraph. Specifically:

> An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, ms though fled on the date of the prior application[.]

(35 U.S.C. 120, Benefit of Earlier Filing Date in the U.S.)

35 U.S.C. 112, 1st paragraph, in turn, requires the written description of the application describe the claimed invention with sufficient particularity that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-17 (Fed. Cir. 1991). See also MPEP § 2163.

Thus, in reexamination, an analysis of the instant Patent's effective priority date is proper.

Analysis

4. Third Party alleges on pp. 11-21 of the request a number of features in the claims that are allegedly not supported by the original disclosure of the '846 parent patent under 35 U.S.C. §112. The references that predate April 10, 2000, for the purposes of this proceeding as it currently stands thus may potentially raise a SNQ over claims of the instant Patent.

The request on page 11, notes that the claims 1-33 and 35-41[1] do not require that the output driver circuitry of the controller device be configured to a multiplexed bus. The requests notes that the multiplexed bus was an essential element of the original disclosure and the input receiver circuitry must be configured to connected to a multiplexed bus. The request notes since the original disclosure requires a multiplex bus and the instant patent is alleged to not require the multiplex bus, then the '8,020 patent is not supported by the original disclosure of the '846

[1] The Examiner notes that the request states that there is lack of support for claims 1-41, however only claims 30-33,35-36 and 38-41 were requested.

parent patent. The request notes that in section 2163.05(I) of the MPEP "under certain circumstances, omission of a limitation can raise an issue regarding whether the inventor had possession of a broader, more generic invention", and "a claim that omits an element which the applicant describes as an essential or critical feature of the invention originally discloses does not comply with the written description requirement.' See pages 11-17 for additional comments, with respect to the "multiplexed bus" made by the requester, which is hereby incorporated by reference.

The request on page 17, notes that the '846 parent patent does not provide support for "transmitting operation codes in any way other than as parameters of a packet on a multiplexed bus" as required by claims 1-. See pages 17-18 for comments, with respect to the "transmitting operation codes" limitation made by the requester, which is hereby incorporated by reference.

The request on page 18, notes that the '846 parent patent does not provide support for an external signal line that is not a multiplexed bus. See page 18 for comments, with respect to the "an external signal line that is not a multiplexed bus" limitation made by the requester, which is hereby incorporated by reference.

The request on page 18, notes that the '846 parent patent does not support claims 1-41 if they do not require two external clock signals. See pages 18-19 for comments, with respect to the "requirement of two external clock signals" limitation made by the requester, which is hereby incorporated by reference.

The request on page 18 notes that the '846 parent patent does not support inputting or outputting data or control information on the transition of an external clock signal as required by claims 1-41 of the '8020 patent. See pages 19-20 for comments, with respect to the "inputting or

outputting data or control information on the transition of an external clock signal" limitation made by the requester, which is hereby incorporated by reference.

The request on page 20, notes that the '846 parent patent does not support a delay locked loop as required by claim 4. See page 20 for comments, with respect to the "delay locked loop" limitation made by the requester, which is hereby incorporated by reference.

Based on this issue, a question is raised as to whether or not the claims are supported by the '846 parent patent, thus the references that predate the filing date of this instant patent, for the purpose of this proceeding as it currently stands, raises a SNQ over the claims of the instant Patent.

Prosecution History

During the prosecution of the 09/545,648 application, the Applicant, in response to the office action mailed on September 11, 2000, file a response on October 2, 2000, which amended at least one claim in response a single means rejection. The application was subsequently allowed and no apparent reasons for allowance were set forth by the Examiner.

Discussion of References that Raise a SNQ

Claim 30 is representative:

An integrated circuit device comprising:
input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; and
output driver circuitry to output data in response to the operation code, wherein:
the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and
the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

Issue 1

The request alleges that a SNQ is raised by the **JEDEC Standard** reference.

The JEDEC Standard reference was cited during prosecution of the Farmwald et al. patent, but was not applied during prosecution in a rejection of a claim. Thus, a substantial new question of patentability would facially be based on patents and/or printed publications already cited/considered in an earlier concluded examination of the patent being reexamined. However, on November 2, 2002, Public Law 107-273 was enacted. Title III, Subtitle A, Section 13105, part (a) of the Act revised the reexamination statute by adding the following new last sentence to 35 U.S.C. 303(a) and 312(a):

> "The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office."

For any reexamination ordered on or after November 2, 2002, the effective date of the statutory revision, reliance on previously cited/considered art, i.e., "old art," does not necessarily preclude the existence of a substantial new question of patentability (SNQ) that is based exclusively on that old art. Rather, determinations on whether a SNQ exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis.

A discussion of the specifics now follows:

The JEDEC Standard defines design parameters for an integrated circuit device comprising a Synchronous Dynamic Random Access Memory (SDRAM), (Section 3.1 1). The JEDEC Standard also describes integrated circuits with input pins and circuitry for receiving

control signals/S, /RE, /CE, and/W signals (page 3.1 1.6-12 discusses "control circuits" for receiving control signals). These control signals are used to instruct the memory device to perform a Read operation, (Table 3.11.5.1-1 lists the states of operation of the memory device, including a read operation). The control signals are also synchronously received at the transition of the external clock signal CK. See the timing diagram at section 3.11.5.1.16.

The JEDEC Standard describes various timing diagrams throughout its disclosure to show output data being driven by the memory device onto the DQn pins. Specifically, the timing diagram at Section 3.11.5.1.16 illustrates the output of data in response to a burst read command. The JEDEC Standard teaches "driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM .

See also claim chart exhibit J of the request.

The teaching of output driver circuitry outputting a first portion of data in response to a rising edge transition of the external clock signal a second portion of data in response to a falling edge transition of the external clock signal was not considered or discussed on the record during the prosecution of the application which became the '8,020 patent. Therefore, it is agreed that JEDEC standard, when considered in this new light, raises a SNQ over at least claims 30-33, 35-36 and 38-41 of the instant '8,020 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. As discussed above, the priority date of the instant patent is

in question and as such the JEDEC Standard reference presents a date of filing or publication which may predate the instant filing date. Accordingly the JEDEC Standard reference raises a SNQ as to at least claims 30-33, 35-36 and 38-41 of the instant '8,020 Patent.

Issue 2

The request alleges that a SNQ is raised by the **Hynix-1** reference.

Hynix -1 discloses a SDRAM memory device that has a plurality of memory cells, (pages 1,3). The Hyundai HY57V651622 is a 67,108,864-bit CMOS Double Data Rate (DDR) Synchronous DRAM. Hynix -1 also discloses a SDRAM memory device that processes control signals that designates a read operation, (page 8 - Simplified Command Truth Table. Input receiver circuitry is shown in the block diagram at pg. 3. The disclosed SDRAM memory device receives the read command (operation code) on pins/ CAS, /RAS, /WE, and/CS, (pages 2 and 8).

HY57V651622 is offering fully synchronous operation referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock, (page 1). Output driver circuitry is shown in the block diagram at pg. 3. A read operation is defined by a certain set of control signals in the Command Truth Table that instructs the device to output data from the memory device, (page 8). Hynix -1 discloses an SDRAM memory device receiving a read command (the operation code) that instructs the memory device to output data, (pages 1 and 8). Data(DQ)..are sampled on both rising and falling edges of [the clock], (page 1).

The teaching of output driver circuitry outputting a first portion of data in response to a rising edge transition of the external clock signal a second portion of data in response to a falling

edge transition of the external clock signal was not considered or discussed on the record during the prosecution of the application which became the '8,020 patent and thus it is agreed that Hynix-1 raises an SNQ over at least claims 30-32, 35-36 and 38 of the instant '8,020 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Furthermore, the Hynix-1 reference was not before the examiner during the prosecution of the '8,020 Patent. Lastly, as discussed above, the priority date of the instant patent is in question and as such the Hynix-1 reference presents a date of filing or publication which may predate the instant filing date. Accordingly, the Hynix-1 reference raises a SNQ as to at least claims 30-32, 35-36 and 38 of the instant '8,020 Patent.

Issue 3

The request alleges that a SNQ is raised by the **Park in view of JEDEC.**

Park discloses a semiconductor memory and, more particularly, to a synchronous dynamic random access memory which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU), (col. 1, lines 9-14). Park describes input receiver circuitry that receives control signals. Commands, such as a read command, are sent by using control signals (e.g.,/RAS,/CAS, /WE,/CS). For a read command,/RAS is high,/CAS is low and/WE is high. After the activation, at the leading edge of the system clock CLK, the high level /RAS, the low level/CAS and the high level/WE indicate a read command, (col. 12, lines 13-15; fig. 5a). The serial data outputs via corresponding data output buffer to data input/output pads in synchronism

with a system clock. Therefore, the 8-bit parallel data continuously outputs every clock cycle thereof, (col. 11, lines 22-26; figs 23, 26 and 57).

Park discloses a synchronous DRAM that outputs data to a bus synchronous to a rising transition of an external clock. Specifically, it can be seen that the first data is generated at the rising edge of the third clock of the system clock CLK after the activation of CAS/, and continuous 4-bit data is outputted in synchronism with the system clock CLK, (col. 40, lines 12-16).

In addition, the JEDEC Standard describes a memory device capable of outputting and sampling data on rising and falling edge transitions of an external clock signal. That is, driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM, (Section 3.11.5.2.1).

See also claim chart exhibit K of the request.

The teaching of output driver circuitry outputting a first portion of data in response to a rising edge transition of the external clock signal a second portion of data in response to a falling edge transition of the external clock signal was not considered or discussed on the record during the prosecution of the application which became the '8,020 patent and thus it is agreed that Park in view of JEDEC raises a SNQ over at least claims 30-33, 35-36 and 38 of the instant '8,020 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims

under reexamination are patentable. Furthermore, the Park in view of JEDEC references were not before the examiner during the prosecution of the '8,020 Patent. Lastly, as discussed above, the priority date of the instant patent is in question and as such the Park in view of JEDEC references presents a date of filing or publication which may predate the instant filing date. Accordingly, the Park in view of JEDEC references raises a SNQ as to at least claims 30-33, 35-36 and 38 of the instant '8,020 Patent.

Issues 4-6, 9 and 10

The request alleges that several SNQs are raised by the **iAPX Manual.**

The iAPX Manual describes the iAPX 432 system, (page 1-2). The iAPX Manual describes a synchronous memory module formed by the combination of a memory control unit (MCU) and its associated storage array, (figure 1-2 - page 1-3). The MCU is a synchronous device that communicates over the memory (MACD) bus using message packets, including a Memory Read Request message packet, (pages F-2 and F-5). A "read operation" is specified by an operation code, (page F-5). The operation code, as part of the Memory Read Request message packet, is sampled synchronously with respect to external clock signal CLKA from the MACD bus. When the operation code bits [15:12] of a message packet are set to "0000", this specifies that the requested operation is a Memory Read Request message packet, (page F-5).

These bits are sampled in the first bus cycle (T-0), (page F-5). The MCU includes two clock inputs: CLKA and CLKB, (page 5-21 - Table 5-6). In one example, the memory bus operates at a clock speed of 5 MHz, (pages C-25; Table F-1 at pg. F-5 shows the message format for message packets sent on the clocked memory bus).

IN addition, the iAPX Specification reference at pages MCU-17, MCU-19, and MCU-36 further show that the bits read from the MACD bus are sampled on the rising edge of CLKA.

In response to a Memory Read Request, the MCU of the memory module outputs data ("DataAB(n)") onto the MACD bus in the form of a "Memory Bus Reply Message". Specifically, the output drivers output the read data onto the MACD bus, (figures 1-2, page 1-3). These output drivers receive data from the MACD bus and are part of the error checking scheme. The loopback check on the memory modules must all be operating correctly, and those drivers on the back-up bus must all be turned off....he TTL buffers, which isolate the MCUs from each memory bus, can be activated only if both MCUs agree on which bus to activate, (pages 4-8).

Table 5-6 shows two input clock pins CLKA and CLKB, (page 5-21). The MACD bus is synchronous, and includes two clock signals - CLKA and CLKB. See Table 5-6, pg. 5-21 of the iAPX Manual. The values output by the memory module are output with respect to an external clock signal. See also, the iAPX Specification which discloses that the read output data is output onto the MACD bus synchronously with respect to the rising edge of CLKB, (pages MCU 16, MCU- 19, MCU-36). The iAPX Specification provides detail of both the BIU and the MCU, including the hardware configuration figure showing a memory read operation, (page BIU-17).

In addition, Inagaki teaches a semiconductor memory device that has an external clock signal φ1 that is used to generate two internal clock signals φ1 and φ2. The two internal clock signals φ1 and φ2 are driven by the rising and falling transitions of the external clock signal φ. The rise and fall of the external clock φ are detected, and clocks φ1 and φ2 are generated. The operating speed is twice that of the conventional speed. The data output buffer of Inagaki has two circuits, each receiving one of the two internal clock signals φl and φ2, so that input data can

be received at twice the data rate as the external clock. The block access memory of the present invention may also form each of the I/O shift register, data input buffer, and data output buffer to two circuits in parallel, which are connected so as to be driven offset by a half-cycle from each other... The operating speed is twice that of the conventional speed. Inagaki provides for generating two internal clock signals φl and φ2, which are used to input data at twice the data rate.

See also claim chart exhibit L of the request.

The teaching of output driver circuitry outputting a first portion of data in response to a rising edge transition of the external clock signal a second portion of data in response to a falling edge transition of the external clock signal was not present in the prosecution of the application which became the '8,020 patent and thus it is agreed that iAPX Manual, iAPX Specification and Inagaki raises an SNQ over at least claims 30-33,35-36 and 38-41 of the instant '8,020 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Furthermore, the iAPX Manual, iAPX Specification and the Inagaki reference were not before the examiner during the prosecution of the '8,020 patent. Accordingly the iAPX Manual, iAPX Specification and the Inagaki raises a SNQ as to at least claims 30-33, 35-36 and 38-41 of the instant '020 Patent.

Issues 7,8,11 and 12

The request alleges that several SNQs are raised by US Patent 4,480,307 to **Budde et al.**

Budde describes a synchronous memory device including, in combination, a "memory control unit 102" and a "memory module 112," connected by the "SLAD" bus and "CNTRL" bus, (figure 1). The MCU receives variable-length access requests at its memory bus interface from a bus interface unit on the MACD bus and makes the proper series of accesses to memory through its storage bus interface. After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus. The operation codes are received by the memory device on the MACD bus within a packet and sampled with respect to a transition of external clock signal CLKB. Packets comprising one or more bus transmission slots are issued sequentially and contiguously. Each slot in a packet includes an opcode, address, data, control, and parity-check bits. Write -request packets and read-request packets are issued to the memory-control unit, (col. 2, lines 21-32). Read requests are received by the memory device on the MACD bus within a packet and sampled with respect to a transition of external clock signal CLKB. In response to a Memory Read Request, the memory device outputs read data in the form of a Read Reply onto the MACD bus. The MCU receives variable-length access requests at its memory bus interface from a bus interface unit on the MACD bus and makes the proper series of accesses to memory through its storage bus interface. After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus, (col. 9, lines 46-54). Typical operation involves time-multiplexing data on these lines in the following order: Control information for bus transactions, address information for the operation requested, data requested by the preceding address and control, (col. 6, lines 43-47). After completion of the accesses to memory, the MCU returns the proper reply on the MACD bus, (col. 9, lines 52-54).This reply is

the normal reply issued in response to one of the following requests: MCU to bus interface unit--Memory Read Request, (col. 13, lines 46-54).

In addition, data is output on the rising edge of CLKB. "CLKA and CLKB provide basic timing references for the BIU and MCU. CLKB lags CLKA by (nominally) 1/4 cycle (90 degrees). Arbitration related signals are driven with CLKA falling, and sampled with CLKA falling. MACD [15:0] is driven and sampled with CLKB rising (3/4 cycle timing). Buffer directional control for the memory bus is altered with CLKA rising, (col. 7, lines 12-19).

In addition, Inagaki teaches a semiconductor memory device that has an external clock signal φ1 that is used to generate two internal clock signals φ1 and φ2. The two internal clock signals φ1 and φ2 are driven by the rising and falling transitions of the external clock signal φ. The rise and fall of the external clock φ are detected, and clocks φ1 and φ2 are generated. The operating speed is twice that of the conventional speed. The data output buffer of Inagaki has two circuits, each receiving one of the two internal clock signals φl and φ2, so that input data can be received at twice the data rate as the external clock. The block access memory of the present invention may also form each of the I/O shift register, data input buffer, and data output buffer to two circuits in parallel, which are connected so as to be driven offset by a half-cycle from each other... The operating speed is twice that of the conventional speed. Inagaki provides for generating two internal clock signals φl and φ2, which are used to input data at twice the data rate.

See also claim chart exhibit M of the request.

The teaching of output driver circuitry outputting a first portion of data in response to a rising edge transition of the external clock signal a second portion of data in response to a falling

edge transition of the external clock signal was not present in the prosecution of the application which became the '8,020 patent and thus it is agreed that Budde and Inagaki raises an SNQ over at least claims 30-33,35-36 and 38-41 of the instant '8,020 Patent.

Thus, given the above teachings, there is a substantially likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the instant claims under reexamination are patentable. Furthermore, the Budde and Inagaki reference were not before the examiner during the prosecution of the '8,020 patent. Accordingly the Budde and Inagaki reference raises a SNQ as to at least claims 30-33,35-36 and 38-41 of the instant '8,020 Patent.

Scope of Reexamination

5. Since requester did not request reexamination of claims 1-29,34 and 37 and did not assert the existence of a substantial new question of patentability (SNQP) for such claims (see 35 U.S.C. § 311(b)(2); see also 37 CFR 1.915b and 1.923), such claims will not be reexamined. This matter was squarely addressed in *Sony Computer Entertainment America Inc., et al. v. Jon W. Dudas*, Civil Action No. 1:05CV1447 (E.D.Va. May 22, 2006), Slip Copy, 2006 WL 1472462. (Not Reported in F.Supp.2d.) The District Court upheld the Office's discretion to not reexamine claims in an *inter partes* reexamination proceeding other than those claims for which reexamination had specifically been requested. The Court stated:

> To be sure, a party may seek, and the PTO may grant, *inter partes* review of each and every claim of a patent. Moreover, while the PTO in its discretion may review claims for which *inter partes* review was not requested, nothing in the statute compels it to do so. To ensure that the PTO considers a claim for *inter partes* review, § 311(b)(2) requires that the party seeking reexamination demonstrate why the PTO should reexamine each and every claim for which it seeks review. Here, it is undisputed that Sony did not seek review of every claim

> under the '213 and '333 patents. Accordingly, Sony cannot now claim that the PTO wrongly failed to reexamine claims for which Sony never requested review, and its argument that AIPA compels a contrary result is unpersuasive.

(Slip copy at page 9.)

The *Sony* decision's reasoning and statutory interpretation apply analogously to *ex parte* reexamination, as the same relevant statutory language applies to both *inter partes* and *ex parte* reexamination. 35 U.S.C. § 302 provides that the *ex parte* reexamination "request must set forth the pertinency and manner of applying cited prior art to every claim for which reexamination is requested" (emphasis added), and 35 U.S.C. § 303 provides that "the Director will determine whether a substantial new question of patentability affecting any claim of the patent concerned is raised by the request..." (Emphasis added). These provisions are analogous to the language of 35 U.S.C. § 311(b)(2) and 35 U.S.C. § 312 applied and construed in *Sony*, and would be construed in the same manner. As the Director can decline to reexamine non-requested claims in an *inter partes* reexamination proceeding, the Director can likewise do so in *ex parte* reexamination proceeding. See *Notice of Clarification of Office Policy To Exercise Discretion in Reexamining Fewer Than All the Patent Claims* (signed Oct. 5, 2006) 1311 OG 197 (Oct. 31, 2006). See also MPEP § 2240, Rev. 5, Aug. 2006.

Therefore, claims 1-29,34 and 37 will not be reexamined in this *inter partes reexamination* proceeding.

For the reasons set forth *supra*, the request raises an SNQ as to claims 30-33, 35-36 and 38-41 of the instant 6,378,020 Patent to Farmwald et al. The request for *inter partes* reexamination is Granted.

Claims 30-33,35-36 and 38-41 of U.S. Patent 6,378,020 will be reexamined.

Conclusion

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

6. Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes* reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant"

and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c) requires that inter partes reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.937). Patent owner extensions of time in inter partes reexamination proceedings are provided for in 37 CFR 1.956. Extensions of time are not available for third party requester comments, because a comment period of 30 days from service of patent owner's response is set by statute. 35 U.S.C. 314(b)(3).

7. The Patent Owner is reminded of the continuing responsibility under 37 CFR 1.985(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the US Patent 6,378,020 throughout the course of this reexamination proceeding. The Third Party Requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding through the course of this reexamination proceeding. See MPEP § 2686 and 2686.04.

8. All correspondence relating to this *inter partes* reexamination proceeding should be directed as follows:

By **U.S. Postal Service Mail** to:

Mail Stop *Inter Partes* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building

401 Dulany St.
Alexandria, VA 22314

9. Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Ovidio Escalante

Ovidio Escalante
Primary Examiner
Central Reexamination Unit 3992

Conferee:

Conferee: